Fraunhofer IPMS

Low Latency Ethernet Media Access Controller

LLEMAC-1G

The LLEMAC-1G is an Ethernet media access controller core that is compatible with the 10/100/1000 Mbps IEEE 802.3 and 1 Gbps IEEE 802.3-2002 specifications. The core offers extremely low input and output latency, making it ideal for implementation in Ethernet TSN nodes and other devices that require very low latency when receiving and sending Ethernet frames.

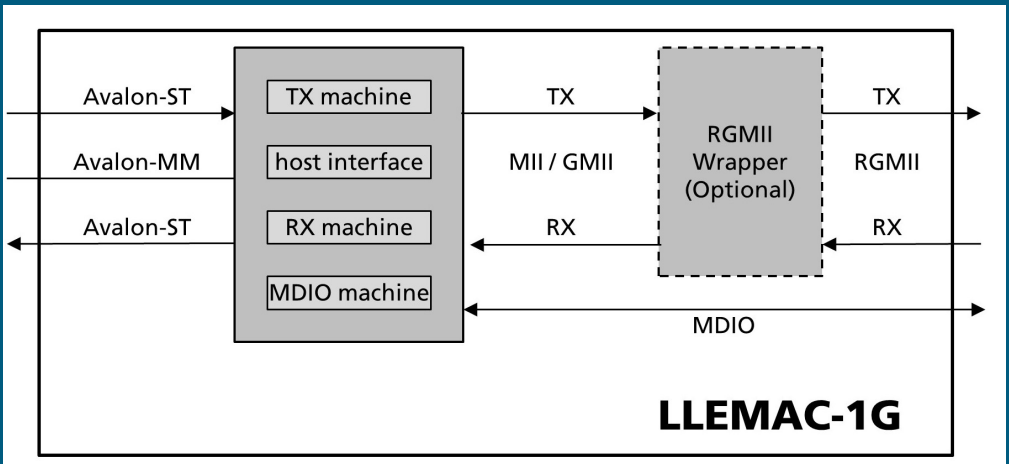
LLEMAC-1G is ready for functional safe system development according to ISO 26262 “Road vehicles – Functional safety”. ISO 26262 defines automotive safety integrity levels (ASIL) and LLEMAC-1G has been certified as “ASIL D ready” by the world’s leading testing, inspection and certification company SGS TÜV Saar GmbH. Therefore a safety enhanced version of the core is available, which implements clock activity monitors and utilizes spatial redundancy. DMR (dual mode redundancy) and DMR-LS (lockstep) are configurable. To ease the safety certification of systems using LLEMAC-1G FMEDA and SAM are shiped with the safety package.

The core is provided in Verilog RTL or as a targeted FPGA netlist and contains everything needed for a successful implementation, including a test bench, sample scripts, and extensive documentation.

Contact

Monika Beck
+49 351 8823-274
monika.beck@
ipms.fraunhofer.de

Fraunhofer Institute for
Photonic Microsystems IPMS
Maria-Reiche-Str. 2
01109 Dresden
www.ipms.fraunhofer.de



Features

- Triple Speed 10/100/1000 Mbps Low Latency Ethernet MAC
- Supports 10BASE-T1S, 10BASE-T, 100BASE-T and 1000BASE-T operation
- Supports IEEE 802.3
- Enables high-precision synchronization in TSN networks
- Egress latency: 10 Tx clock cycles
- Ingress latency: 6 Rx clock cycles
- Full duplex /Half Duplex point-to-point links

Interfaces

- Media Independent Interface (MII) for 10/100 Mbps
- Gigabit Media Independent Interface (GMII) for 1Gbps
- Reduced Gigabit Media Independent Interface (RGMII) for 10/100/1000 Mbps
- Serial Gigabit Media Independent Interfac (SGMII) for FPGA (for ASIC on request)
- MDIO interface for PHY configuration and management
- Host Interfaces to AXI, Avalon-ST/MM

Easy System Integration

- Platform independent implementation Xilinx, Intel, Microsemi, Lattice, Gowin FPGAs and any foundry technology
- Silicon proven
- Autonomous operation, requires no host assistance once programmed
- Responsive implementation support

Deliverables

- Source code Verilog RTL or targeted netlist
- Testbench
- Sample synthesis and simulation scripts
- Comprehensive documentation

Safety Enhanced Package

- SAM and FDMEA certified ISO-26262 ASIL D ready
- Spatial redundancy for inner logic protection
- ISO-26262 documentation package
- Clock activity monitoring

MACsec IP Core controller

Fraunhofer IPMS offers a MACSec IP Core Controller which is used for authentication and encryption of data packets between ethernet network devices. It can be used with the LLEMAC core or in standalone operations.